AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor memory device comprising:

a plurality of memory cells corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer;

an invalid address detecting circuit ~~for~~ detecting that an address signal supplied from exterior indicates an address space other than said address space;

an invalid signal outputting circuit ~~for~~ outputting an invalid signal via a dedicated terminal to the exterior of the semiconductor memory device when said invalid address detecting circuit carries out said detection; ~~and~~

a latch circuit latching read data read from said memory cells in each read operation; and

an output controlling circuit ~~for~~ outputting, without accessing said memory cells, the read data latched in said latch circuit by the preceding read operation, when said invalid address detecting circuit carries out said detection in a read operation~~, a data signal having been accessed and read in advance~~.

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Currently Amended) A semiconductor memory device comprising:

a plurality of memory cells corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer;

an invalid address detecting circuit ~~for~~ detecting that an address signal supplied from exterior indicates an address space other than said address space; ~~and~~

a latch circuit latching read data read from said memory cells in each read operation; and

an output controlling circuit ~~for~~ outputting, without accessing said memory cells, the read data latched in said latch circuit by the preceding read operation, when said invalid address detecting circuit carries out said detection in a read operation~~, a data signal having been accessed and read in advance~~.

6. (Cancelled)

7. (Currently Amended) A semiconductor memory device according to claim 1, further comprising:

a command controlling circuit ~~for~~ carrying out a write or an erase operation in said memory cells in response to a command input from the exterior, wherein

said command controlling circuit invalidates said command input to thereby prohibit the write or the erase operation, when the invalid address detecting circuit detects that the address signal supplied from exterior as the command input indicates the address space other than the said address space.

8. (Cancelled)

9. (Currently Amended) A method of controlling a semiconductor memory device comprising a plurality of memory cells corresponding to an address space larger than 2^n and ~~small~~ smaller than $2^{(n+1)}$, where n is a positive integer, said method comprising the ~~step~~ steps of:

latching read data read from said memory cells in each read operation; and

outputting an invalid signal via a dedicated terminal to the exterior of the semiconductor memory device ~~and outputting a data signal having been accessed and read in advance~~, and outputting, without accessing said memory cells, the read data latched by the preceding read operation, when an address signal supplied from the exterior indicating an address space other than said address space has been detected.

10. (Previously Presented) A method of controlling a semiconductor memory device according to claim 9, further comprising the steps of:

automatically carrying out a write or an erase operation in said memory cells in response to a command input from the exterior

invalidating the command input thereby prohibiting the write or the erase operation, when the address signal supplied from the exterior indicating the address space other than the said address space has been detected.

11. (Previously Presented) A semiconductor memory device according to claim 1, further comprising:

a decoder which decodes said address signal, and is inactivated when said invalid address detecting circuit carries out said detection.

12. (Previously Presented) A semiconductor memory device according to claim 1, further comprising:

a sense amplifier which amplifies a data signal read from the memory cells, and is inactivated when said invalid address detecting circuit carries out said detection.